

ABSTRACT OF THE INVENTION

The selective etch shallow trench isolation barrier integrated circuit fabrication system and method of the present invention minimizes the layers required to implement a shallow trench isolation barrier in an integrated circuit. A selective etch shallow trench isolation barrier integrated circuit in which a selective etch shallow trench isolation barrier is adjacent to an intermetal dielectric layer. Etching space in the intermetal dielectric layer for a contact plug is performed in a single film layer etch step. The selective etch shallow trench isolation barrier includes selective etch isolation material able to both withstand etching processes directed toward the insulation layer (e.g., to create a space for a contact plug) and facilitate isolation of devices from outside electrical influences. A present invention selective etch shallow trench isolation barrier integrated circuit does not require a shallow trench isolation barrier etch stop layer.

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[VLSI 3397]